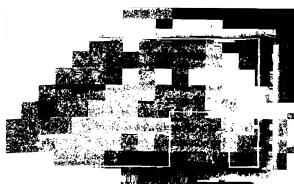


# CONTENTS



List of Tables	xxii	1.6.5 Regulators	34
Preface to the First Edition	xxv	1.6.6 Circuit applications of diodes	35
Preface to the Second Edition	xxvii	1.6.7 Inductive loads and diode protection	38
Preface to the Third Edition	xxix	1.6.8 Interlude: inductors as friends	39
<b>ONE: Foundations</b>	<b>1</b>	<b>1.7 Impedance and reactance</b>	<b>40</b>
1.1 Introduction	1	1.7.1 Frequency analysis of reactive circuits	41
1.2 Voltage, current, and resistance	1	1.7.2 Reactance of inductors	44
1.2.1 Voltage and current	1	1.7.3 Voltages and currents as complex numbers	44
1.2.2 Relationship between voltage and current: resistors	3	1.7.4 Reactance of capacitors and inductors	45
1.2.3 Voltage dividers	7	1.7.5 Ohm's law generalized	46
1.2.4 Voltage sources and current sources	8	1.7.6 Power in reactive circuits	47
1.2.5 Thévenin equivalent circuit	9	1.7.7 Voltage dividers generalized	48
1.2.6 Small-signal resistance	12	1.7.8 RC highpass filters	48
1.2.7 An example: "It's too hot!"	13	1.7.9 RC lowpass filters	50
1.3 Signals	13	1.7.10 RC differentiators and integrators in the frequency domain	51
1.3.1 Sinusoidal signals	14	1.7.11 Inductors versus capacitors	51
1.3.2 Signal amplitudes and decibels	14	1.7.12 Phasor diagrams	51
1.3.3 Other signals	15	1.7.13 "Poles" and decibels per octave	52
1.3.4 Logic levels	17	1.7.14 Resonant circuits	52
1.3.5 Signal sources	17	1.7.15 LC filters	54
1.4 Capacitors and ac circuits	18	1.7.16 Other capacitor applications	54
1.4.1 Capacitors	18	1.7.17 Thévenin's theorem generalized	55
1.4.2 RC circuits: V and I versus time	21	1.8 Putting it all together – an AM radio	55
1.4.3 Differentiators	25	1.9 Other passive components	56
1.4.4 Integrators	26	19.1 Electromechanical devices: switches	56
1.4.5 Not quite perfect...	28	19.2 Electromechanical devices: relays	59
1.5 Inductors and transformers	28	19.3 Connectors	59
1.5.1 Inductors	28	19.4 Indicators	61
1.5.2 Transformers	30	19.5 Variable components	63
1.6 Diodes and diode circuits	31	1.10 A parting shot: confusing markings and bit-by-bit components	64
1.6.1 Diodes	31	1.10.1 Surface-mount technology: the joy and the pain	65
1.6.2 Rectification	31		
1.6.3 Power-supply filtering	32		
1.6.4 Rectifier configurations for power supplies	33		

x	<b>Contents</b>	<i>Art of Electronics Third Edition</i>	
Additional Exercises for Chapter 1	66	2.6.1 Regulated power supply	123
Review of Chapter 1	68	2.6.2 Temperature controller	123
<b>TWO: Bipolar Transistors</b>	<b>71</b>	2.6.3 Simple logic with transistors and diodes	123
2.1 Introduction	71	<b>Additional Exercises for Chapter 2</b>	124
2.1.1 First transistor model: current amplifier	72	Review of Chapter 2	126
2.2 Some basic transistor circuits	73	<b>THREE: Field-Effect Transistors</b>	131
2.2.1 Transistor switch	73	3.1 Introduction	131
2.2.2 Switching circuit examples	75	3.1.1 FET characteristics	131
2.2.3 Emitter follower	79	3.1.2 FET types	134
2.2.4 Emitter followers as voltage regulators	82	3.1.3 Universal FET characteristics	136
2.2.5 Emitter follower biasing	83	3.1.4 FET drain characteristics	137
2.2.6 Current source	85	3.1.5 Manufacturing spread of FET characteristics	138
2.2.7 Common-emitter amplifier	87	3.1.6 Basic FET circuits	140
2.2.8 Unity-gain phase splitter	88	3.2 FET linear circuits	141
2.2.9 Transconductance	89	3.2.1 Some representative JFETs: a brief tour	141
2.3 Ebers-Moll model applied to basic transistor circuits	90	3.2.2 JFET current sources	142
2.3.1 Improved transistor model: transconductance amplifier	90	3.2.3 FET amplifiers	146
2.3.2 Consequences of the Ebers-Moll model: rules of thumb for transistor design	91	3.2.4 Differential amplifiers	152
2.3.3 The emitter follower revisited	93	3.2.5 Oscillators	155
2.3.4 The common-emitter amplifier revisited	93	3.2.6 Source followers	156
2.3.5 Biasing the common-emitter amplifier	96	3.2.7 FETs as variable resistors	161
2.3.6 An aside: the perfect transistor	99	3.2.8 FET gate current	163
2.3.7 Current mirrors	101	3.3 A closer look at JFETs	165
2.3.8 Differential amplifiers	102	3.3.1 Drain current versus gate voltage	165
2.4 Some amplifier building blocks	105	3.3.2 Drain current versus drain-source voltage: output conductance	166
2.4.1 Push-pull output stages	106	3.3.3 Transconductance versus drain current	168
2.4.2 Darlington connection	109	3.3.4 Transconductance versus drain voltage	170
2.4.3 Bootstrapping	111	3.3.5 JFET capacitance	170
2.4.4 Current sharing in paralleled BJTs	112	3.4.1 Why JFET (versus MOSFET) amplifiers?	170
2.4.5 Capacitance and Miller effect	113	3.4 FET switches	171
2.4.6 Field-effect transistors	115	3.4.1 FET analog switches	171
2.5 Negative feedback	115	3.4.2 Limitations of FET switches	174
2.5.1 Introduction to feedback	116	3.4.3 Some FET analog switch examples	182
2.5.2 Gain equation	116	3.4.4 MOSFET logic switches	184
2.5.3 Effects of feedback on amplifier circuits	117	3.5 Power MOSFETs	187
2.5.4 Two important details	120	3.5.1 High impedance, thermal stability	187
2.5.5 Two examples of transistor amplifiers with feedback	121	3.5.2 Power MOSFET switching parameters	192
2.6 Some typical transistor circuits	123		

xii	<b>Contents</b>	<i>Art of Electronics Third Edition</i>	
5.4 Another example: precision amplifier with null offset	297	5.11.3 Selecting an auto-zero op-amp	338
5.4.1 Circuit description	297	5.11.4 Auto-zero miscellany	340
5.5 A precision error budget	298	<b>5.12 Designs by the masters: Agilent's accurate DMAs</b>	342
5.5.1 Error budget	299	5.12.1 It's impossible!	342
5.6 Component errors	299	5.12.2 Wrong – it is possible!	342
5.6.1 Gain-setting resistors	300	5.12.3 Block diagram: a simple plan	343
5.6.2 The holding capacitor	300	5.12.4 The 34401A 6.5-digit front end	343
5.6.3 Nulling switch	300	5.12.5 The 34420A 7.5-digit frontend	344
5.7 Amplifier input errors	301	<b>5.13 Difference, differential, and instrumentation amplifiers: introduction</b>	347
5.7.1 Input impedance	302	5.14 Difference amplifier	348
5.7.2 Input bias current	302	5.14.1 Basic circuit operation	348
5.7.3 Voltage offset	303	5.14.2 Some applications	349
5.7.4 Common-mode rejection	305	5.14.3 Performance parameters	352
5.7.5 Power-supply rejection	306	5.14.4 Circuit variations	355
5.8 Amplifier output errors	307	<b>5.15 Instrumentation amplifier</b>	356
5.8.1 Slew rate: general considerations	307	5.15.1 A first (but naive) guess	357
5.8.2 Bandwidth and settling time	308	5.15.2 Classic three-op-amp instrumentation amplifier	357
5.8.3 Crossover distortion and output impedance	309	5.15.3 Input-stage considerations	358
5.8.4 Unity-gain power buffers	311	5.15.4 A "roll-your-own" instrumentation amplifier	359
5.8.5 Gain error	312	5.15.5 A riff on robust input protection	362
5.8.6 Gain nonlinearity	312	5.16 Instrumentation amplifier miscellany	362
5.8.7 Phase error and "active compensation"	314	5.16.1 Input current and noise	362
5.9 RRIOPs: the good, the bad, and the ugly	315	5.16.2 Common-mode rejection	364
5.9.1 Input issues	316	5.16.3 Source impedance and CMRR	365
5.9.2 Output issues	316	5.16.4 EMI and input protection	365
5.10 Another look at precision op-amps	319	5.16.5 Offset and CMRR trimming	366
5.10.1 "Open-loop" precision op-amps	319	5.16.6 Sensing at the load	366
5.10.2 Number per package	322	5.16.7 Input bias paths	366
5.10.3 Supply voltage, signal range	322	5.16.8 Output voltage range	367
5.10.4 Single-supply operation	322	5.16.9 Application example: current source	367
5.10.5 Offset voltage	323	5.16.10 Other configurations	368
5.10.6 Voltage noise	323	5.17 Differential amplifiers: basic concepts	374
5.10.7 Bias current	325	5.17.1 Differential amplifiers	370
5.10.8 Current noise	326	5.17.2 Differential amplifier application example: wideband analog link	380
5.10.9 CMRR and PSRR	328	5.17.3 Differential-input ADCs	380
5.10.10 GBW <sub>f</sub> , slew rate and "m,"	328	5.17.4 Impedance matching	382
5.10.11 Settling time	329		
5.10.12 Distortion	329		
5.10.13 "Two out of three isn't bad": creating a perfect op-amp	332		
5.11 Auto-zeroing (chopper-stabilized) amplifiers	333		
5.11.1 Auto-zero op-amp properties	334		
5.11.2 When to use auto-zero op-amps	338		
5.11.3 Generating a differential output	372		
5.11.4 Fully differential amplifiers	373		
5.11.5 Differential amplifiers: basic concepts	374		

5.17.5 Differential amplifier selection criteria	383	7.2.4 Timing with digital counters	465
Review of Chapter 5	388	Review of Chapter 7	470
<b>EIGHT: Low-Noise Techniques</b>			
6.1 Introduction	391	8.1 "Noise"	473
6.2 Passive filters	391	8.1.1 Johnson (Nyquist) noise	474
6.2.1 Frequency response with $RC$ filters	391	8.1.2 Shot noise	475
6.2.2 Ideal performance with $LC$ filters	391	8.1.3 $1/f$ noise (flicker noise)	476
6.2.3 Several simple examples	393	8.1.4 Power-limited noise	477
6.2.4 Extractive filters: an overview	396	8.1.5 Band-limited noise	477
6.2.5 Key filter performance criteria	399	8.1.6 Interference	478
6.2.6 Filter types	400	8.2 Signal-to-noise ratio and noise figure	478
6.2.7 Filter implementation	405	8.2.1 Noise power density and bandwidth	479
6.3 Active-filter circuits	406	8.2.2 Signal-to-noise ratio	479
6.3.1 VCVS circuits	407	8.2.3 Noise figure	479
6.3.2 VCVS filter design using our simplified table	407	8.2.4 Noise temperature	480
6.3.3 State-variable filters	410	8.3 Bipolar transistor amplifier noise	481
6.3.4 Twin-T notch filters	414	8.3.1 Voltage noise, $\epsilon_v$	481
6.3.5 Allpass filters	415	8.3.2 Current noise $i_n$	483
6.3.6 Switched-capacitor filters	415	8.3.3 BJT voltage noise, revisited	484
6.3.7 Digital signal processing	418	8.3.4 A simple design example: loudspeaker as microphone	486
6.3.8 Filter miscellany	422	8.3.5 Shot noise in current sources and emitter followers	487
Additional Exercises for Chapter 6	422	8.4 Finding $\epsilon_v$ from noise-figure specifications	489
Review of Chapter 6	423	8.4.1 Step 1: NF versus $i_n$	489
SEVEN: Oscillators and Timers	425	8.4.2 Step 2: NF versus $R_s$	489
7.1 Oscillators	425	8.4.3 Step 3: getting to $\epsilon_v$	490
7.1.1 Introduction to oscillators	425	8.4.4 Step 4: the spectrum of $\epsilon_v$	491
7.1.2 Relaxation oscillators	425	8.4.5 When operating current is not your choice	491
7.1.3 The classic oscillator-timer chip: the 555	428	8.5 Low-noise design with bipolar transistors	492
7.1.4 Other relaxation-oscillator ICs	432	8.5.1 Noise-figure example	492
7.1.5 Sinewave oscillators	435	8.5.2 Charting amplifier noise with $\epsilon_v$ and $i_n$	493
7.1.6 Quartz-crystal oscillators	443	8.5.3 Noise resistance	494
7.1.7 Higher stability: TCXO, OCXO, and beyond	450	8.5.4 Charting comparative noise	495
7.1.8 Frequency synthesis: DDS and PLL	451	8.5.5 Low noise design with BJTs: two examples	495
7.1.9 Quadrature oscillators	453	8.5.6 Minimizing noise: BJTs, FETs, and transformers	496
7.1.10 Oscillator "jitter"	457	8.5.7 A design example: 40 $\mu$ s "lightning-detector" preamp	497
7.2 Timers	457	8.5.8 Selecting a low-noise bipolar transistor	500
7.2.1 Step-triggered pulses	458	8.5.9 An extreme low-noise design challenge	505
7.2.2 Monostable multivibrators	461		
7.2.3 A monostable application: limiting pulse width and duty cycle	465		

8.6 Low-noise design with JFETs	509	8.11.13 Test fixture for compensation and calibration	554
8.6.1 Voltage noise of JFETs	509	8.11.14 A final remark	555
8.6.2 Current noise of JFETs	511	8.12 Noise measurements and noise sources	555
8.6.3 Design example: low-noise wideband JFET "hybrid" amplifiers	512	8.12.1 Measurement without a noise source	555
8.6.4 Designs by the masters: SR560 low-noise preamplifier	512	8.12.2 An example: transistor-noise test circuit	556
8.6.5 Selecting low-noise JFETs	515	8.12.3 Measurement with a noise source	556
8.7 Charting the bipolar-FET shootout	517	8.12.4 Noise and signal sources	558
8.7.1 What about MOSFETs?	519	8.13 Bandwidth limiting and rms voltage measurement	561
8.8 Noise in differential and feedback amplifiers	521	8.13.1 Limiting the bandwidth	561
8.9 Noise in operational amplifier circuits	521	8.13.2 Calculating the integrated noise	563
8.9.1 Guide to Table 8.3: choosing low-noise opamps	525	8.13.3 Op-amps vs frequency noise	564
8.9.2 Power-supply rejection ratio	525	8.13.4 Finding the $1/f$ corner frequency	566
8.9.3 Wrapup: choosing a low-noise op-amp	533	8.13.5 Measuring the noise voltage	567
8.9.4 Low-noise instrumentation amplifiers and video amplifiers	533	8.13.6 Measuring the noise current	569
8.9.5 Low-noise hybrid op-amps	534	8.13.7 Another way: roll-your-own FET/IF instrument	571
8.10 Signal transformers	535	8.13.8 Noise potpourri	574
8.10.1 A low-noise wideband amplifier with transformer feedback	536	8.14 Signal-to-noise improvement by bandwidth narrowing	574
8.11 Noise in transimpedance amplifiers	537	8.14.1 Lock-in detection	575
8.11.1 Summary of the stability problem	537	8.15 Power-supply noise	578
8.11.2 Amplifier input noise	538	8.15.1 Capacitance multiplier	578
8.11.3 The $e_a C$ noise problem	538	8.16 Interference, shielding, and grounding	579
8.11.4 Noise in the transresistance amplifier	539	8.16.1 Interfering signals	579
8.11.5 An example: wideband JFET photodiode amplifier	540	8.16.2 Signal grounds	582
8.11.6 Noise versus gain in the transimpedance amplifier	540	8.16.3 Grounding between instruments	583
8.11.7 Output bandwidth limiting in the transimpedance amplifier	540	Additional Exercises for Chapter 8	588
8.11.8 Composite transimpedance amplifiers	543	Review of Chapter 8	590
8.11.9 Reducing input capacitance: bootstrapping the transimpedance amplifier	543		
8.11.10 Isolating input capacitance: recoding the transimpedance amplifier	547		
8.11.11 Transimpedance amplifiers with capacitive feedback	552		
8.11.12 Scanning tunneling microscope preamplifier	553		
<b>NINE: Voltage Regulation and Power Conversion</b>			
9.1 Tutorial: from zener to series-pass linear regulators	594		
9.1.1 Adding feedback	595		
9.2 Basic linear regulator circuits with the classic 723	598		
9.2.1 The 723 regulator	598		
9.2.2 In defense of the beleaguered 723	600		
9.3 Fully integrated linear regulators	600		
9.3.1 Taxonomy of linear regulator ICs	601		
9.3.2 Three-terminal fixed regulators	601		

9.3.3 Three-terminal adjustable regulators	602	9.7.1 The $ac-to-dc$ input stage	660
9.3.4 317-style regulator: application hints	604	9.7.2 The dc-to-dc converter	662
9.3.5 317-style regulator: circuit examples	608	9.8 A real-world switcher example	665
9.3.6 Lower-dropout regulators	610	9.8.1 Switchers: top-level view	665
9.3.7 True low-dropout regulators	611	9.8.2 Switchers: basic operation	665
9.3.8 Current-reference 3-terminal regulator	611	9.8.3 Switchers: looking more closely	668
9.3.9 Dropout voltages compared	612	9.8.5 Wrapup: general comments on line-powered switching power supplies	672
9.3.10 Dual-voltage regulator circuit example	613	9.8.6 When to use switchers	672
9.3.11 Linear regulator choices	613	9.9 Inverters and switching amplifiers	673
9.3.12 Linear regulator idiosyncrasies	613	9.10 Voltage references	674
9.3.13 Noise and ripple filtering	619	9.10.1 Zener diode	674
9.3.14 Current sources	620	9.10.2 Bandgap ( $V_{BE}$ ) reference	679
9.4 Heat and power design	623	9.10.3 JFET pinch-off ( $V_D$ ) reference	680
9.4.1 Power transistors and heat sinking	624	9.10.4 Floating-gate reference	681
9.4.2 Safe operating area	627	9.10.5 Three-terminal precision references	681
9.5 From ac line-to-line unregulated supply example	628	9.10.6 Voltage reference noise	682
9.5.1 Line-to-line components	629	9.10.7 Voltage references: additional comments	683
9.5.2 Transformers	632	9.11 Commercial power-supply modules	684
9.5.3 de components	633	9.12 Energy storage batteries and capacitors	686
9.5.4 Unregulated split supply – on the bench!	634	9.12.1 Battery characteristics	687
9.5.5 Linear versus switcher: ripple and noise	635	9.12.2 Choosing a battery	688
9.6 Switching regulators and dc-de converters	636	9.12.3 Energy storage in capacitors	688
9.6.1 Linear versus switching converter topologies	636	9.13 Additional topics in power regulation	690
9.6.2 Switching converter topologies	638	9.13.1 Overvoltage crowbars	690
9.6.3 Inductorless switching converters	638	9.13.2 Extending input-voltage range	693
9.6.4 Converters with inductors: the basic non-isolated topologies	641	9.13.3 Foldback current limiting	693
9.6.5 Step-down (buck) converter	642	9.13.4 Outboard pass transistor	695
9.6.6 Step-up (boost) converter	647	9.13.5 High-voltage regulators	695
9.6.7 Inverting converter	648	Review of Chapter 9	699
9.6.8 Comments on the non-isolated converters	649		
9.6.9 Voltage mode and current mode	651	10.1.5 Discrete circuits for gates	711
9.6.10 Coupling with transformers: the basic designs	653	10.1.6 Gate-logic example	712
9.6.11 The flyback converter	655	10.1.7 Insertion-level logic notation	713
9.6.12 Forward converters	656	10.2 Analog integrated circuits: CMOS and Bipolar (TTL)	714
9.6.13 Bridge converters	659	10.2.1 Catalog of common gates	715
9.7 Ac-line-powered ("offline") switching converters	660	10.2.2 IC gate circuits	717
		10.2.3 CMOS and bipolar ("TTL") characteristics	718

10.2.4 Three-state and open-collector devices	720	11.3 An example: pseudorandom byte generator	770
10.3 Combinational logic	722	11.3.1 How to make pseudorandom bytes	771
10.3.1 Logic identities	722	11.3.2 Implementation in standard logic	772
10.3.2 Mintermization and Karnaugh maps	723	11.3.3 Implementation with programmable logic	772
10.3.3 Combinational functions available as ICs	724	11.3.4 Programmable logic – HDL entry	772
10.4 Sequential logic	728	11.3.5 Implementation with a microcontroller	777
10.4.1 Devices with memory: flip-flops	728	11.4 Advice	782
10.4.2 Clocked flip-flops	730	11.4.1 By Technologies	782
10.4.3 Combining memory and gates: sequential logic	734	11.4.2 By User Communities	785
10.4.4 Synchronizer	737	Review of Chapter 11	787
10.4.5 Monostable multivibrator	739		
10.4.6 Single-pulse generation with flip-flops and counters	739		
10.5 Sequential functions available as integrated circuits	740	<b>TWELVE: Logic Interfacing</b>	790
10.5.1 Latches and registers	740	12.1 CMOS and TTL logic interfacing	790
10.5.2 Counters	741	12.1.1 Logic family chronology – a brief history	790
10.5.3 Shift registers	744	12.1.2 Input and output characteristics	794
10.5.4 Programmable logic devices	745	12.1.3 Interfacing between logic families	798
10.5.5 Miscellaneous sequential functions	746	12.1.4 Driving digital logic inputs	802
10.6 Some typical digital circuits	748	12.1.5 Input protection	804
10.6.1 Modules $n$ -counter: a timing example	748	12.1.6 Some comments about logic inputs	805
10.6.2 Multiplexed LED digital display	751	12.1.7 Driving digital logic from comparators or op-amps	806
10.6.3 An $n$ -pulse generator	752	12.2 An aside: probing digital signals	808
10.7 Microprocessor digital design	753	12.3 Comparators	809
10.7.1 Keeping CMOS low power	754	12.3.1 Outputs	810
10.8 Logic pathology	755	12.3.2 Inputs	812
10.8.1 $d$ problems	755	12.3.3 Other parameters	815
10.8.2 Switching problems	756	12.3.4 Other cautions	816
10.8.3 Congenital weaknesses of TTL and CMOS	758	12.4 Driving external digital loads from logic levels	817
Additional Exercises for Chapter 10	760	12.4.1 Positive loads: direct drive	817
Review of Chapter 10	762	12.4.2 Positive loads: transistor assisted	820
		12.4.3 Negative or ac loads	821
ELEVEN: Programmable Logic Devices	764	12.4.4 Protecting power switches	823
11.1 A brief history	764	12.4.5 nMOS LSI interfacing	826
11.2 The hardware	765	12.5 Optoelectronics: emitters	829
11.2.1 The basic PAL	765	12.5.1 Indicators and LEDs	829
11.2.2 The PLA	768	12.5.2 Laser diodes	834
11.2.3 The FPGA	768	12.5.3 Displays	836
11.2.4 The configuration memory	769	12.6 Optoelectronics: detectors	840
11.2.5 Other programmable logic devices	769		
11.2.6 The software	769		

12.6.1 Photodiodes and phototransistors	841	13.2.8 PWM as digital-to-analog converter	888
12.6.2 Photomultipliers	842	13.2.9 Frequency-to-voltage converters	890
12.7 Optocouplers and relays	843	13.2.10 Rate multiplier	890
12.7.1 I: Phototransistor output optocouplers	844	13.2.11 Choosing a DAC	891
12.7.2 II: Logic-output optocouplers	844	13.3 Some DAC application examples	891
12.7.3 III: Gate driver optocouplers	846	13.3.1 General-purpose laboratory example	891
12.7.4 IV: Analog-oriented optocouplers	847	13.3.2 Eight-channel source bipolarity current source	893
12.7.5 V: Solid-state relays (transistor optoisolators)	848	13.3.3 Nanoamp wide-compliance ADCs	894
12.7.6 VI: Solid-state relays (triac/SCR output)	848	13.4 Converter linearity – a closer look	895
12.7.7 VII: ac input optocouplers	851	13.5 Analog-to-digital converters	900
12.7.8 Interrupts	851	13.5.1 Digitizing: aliasing, sampling rate, and sampling depth	900
12.8 Optoelectronics: fiber-optic digital links	852	13.5.2 ADC Technologies	902
12.8.1 TOSLINK	852	13.6 ADCs I: Parallel ("Flash") encoder	903
12.8.2 Versatile Link	854	13.6.1 Modified flash encoders	903
12.8.3 ST/SC glass-fiber modules	855	13.6.2 Driving flash, folding, and RF ADCs	904
12.8.4 Fully integrated high-speed fiber-transceiver modules	855	13.6.3 Undersampling flash-converter example	907
12.9 Digital signals and long wires	856	13.7 ADCs II: Successive approximation	908
12.9.1 On-board interconnections	856	13.7.1 A simple SAR example	909
12.9.2 Intercard connections	858	13.7.2 Variations on successive approximation	909
12.10 Driving Cables	858	13.7.3 An A/D conversion example	910
12.10.1 Coaxial cable	858	13.8 ADCs III: Integrating	912
12.10.2 The right way – I: Far-end termination	860	13.8.1 Voltage-to-frequency conversion	912
12.10.3 Differential-pair cable	864	13.8.2 Single-slope integration	914
12.10.4 RS-232	871	13.8.3 Integrating converters	914
12.10.5 Wrapup	874	13.8.4 Dual-slope integration	914
Review of Chapter 12	875	13.8.5 Analog switches in conversion applications (a detour)	916
<b>THIRTEEN : Digital meets Analog</b>	<b>879</b>	13.8.6 Designs by the masters: Agilent's world-class "multislope" converters	918
13.1 Some preliminaries	879	13.9 ADCs IV: delta-sigma	922
13.1.1 The basic performance parameters	879	13.9.1 A simple delta-sigma for our suntan monitor	922
13.1.2 Codes	880	13.9.2 Demystifying the delta-sigma converter	923
13.1.3 Converter errors	880	13.9.3 $\Delta\Sigma$ ADC and DAC	923
13.1.4 Stand-alone versus integrated	880	13.9.4 The $\Delta\Sigma$ process	924
13.2 Digital-to-analog converters	881	13.9.5 An aside: "noise shaping"	927
13.2.1 Resistor-string DACs	881	13.9.6 The bottom line	928
13.2.2 R-2R ladder DACs	882	13.9.7 A simulation	928
13.2.3 Current-steering DACs	883	13.9.8 What about DACs?	930

13.9.9 Pros and Cons of $\Delta\Sigma$ oversampling converters	931	13.14.8 A "hybrid digital filter"	983
13.9.10 Idle tones	932	Additional Exercises for Chapter 13	984
13.9.11 Some delta-sigma application examples	932	Review of Chapter 13	985
13.10 ADCs: choices and tradeoffs	932	<b>FOURTEEN: Computers, Controllers, and Data Links</b>	<b>989</b>
13.10.1 Delta-sigma and noise competition	938	14.1 Computer architecture: CPU and data bus	990
13.10.2 Sampling versus averaging ADCs: noise	940	14.1.1 CPU	990
13.10.3 Some unusual A/D and D/A converters	941	14.1.2 Memory	991
13.11 Some unusual A/D and D/A converters	942	14.1.3 Main memory	991
13.11.1 AD7753 multifunction ac power metering IC	943	14.1.4 Graphics, network, parallel, and serial I/O	992
13.11.2 AD7873 touchscreen digitizer	944	14.1.5 Real-time I/O	992
13.11.3 AD7927 ADC with sequencer	945	14.1.6 Data bus	992
13.11.4 AD7730 precision bridge-measurement subsystem	945	14.2 A computer instruction set	993
13.12 Some A/D conversion system examples	946	14.2.1 Assembly language and machine language	993
13.12.1 Multiplexed 16-channel data-acquisition system	946	14.2.2 Simplified "86" instruction set	996
13.12.2 Parallel multichannel delta-sigma data-acquisition system	946	14.2.3 A programming example	996
13.13 Phase-locked loops	955	14.3 Bus signals and interfacing	997
13.13.1 Introduction to phase-locked loops	955	14.3.1 Fundamental bus signals: data, address, strobe	997
13.13.2 PLL components	957	14.3.2 Programmed I/O: data out	998
13.13.3 PLL design	960	14.3.3 Programming the XY vector	1000
13.13.4 Design example: frequency multiplier	961	14.3.4 Programmed I/O: data in	1001
13.13.5 PLL capture and lock	964	14.3.5 Programmed I/O: status registers	1002
13.13.6 Some PLL applications	966	14.3.6 Programmed I/O: command registers	1004
13.13.7 Wrapup: noise and jitter rejection in PLLs	974	14.3.7 Interrupts	1005
13.14 Pseudorandom bit sequences and noise generation	974	14.3.8 Interrupt handling	1006
13.14.1 Digital-noise generation	974	14.3.9 Interrupts in general	1008
13.14.2 Feedback shift register sequences	975	14.3.10 Direct memory access	1010
13.14.3 Analog noise generation from pseudorandom sequences	975	14.3.11 Summary of PC104/ISA 8-bit bus signals	1012
13.14.4 Power spectrum of shift-register sequences	977	14.3.12 The PC104 as an embedded single-board computer	1013
13.14.5 Low-pass filtering	979	14.4 Memory types	1014
13.14.6 Wrapup	981	14.4.1 Volatile and non-volatile memory	1014
13.14.7 "True" random noise generators	982	14.4.2 Static versus dynamic RAM	1015
		14.4.3 Dynamic RAM	1016
		14.4.4 Nonvolatile memory	1021
		14.4.5 DRAM	1026
		14.4.6 Memory wrapup	1027
		14.5 Other buses and data links: overview	1027
		14.6 Parallel buses and data links	1028
		14.6.1 Parallel chip "bus" interface – an example	1028

14.6.2 Parallel chip-data links – two high-speed examples	1030	15.7 Design example 5: stabilized mechanical platform	1077
14.6.3 Other parallel computer buses	1030	15.8 Peripheral ICs for microcontrollers	1078
14.6.4 Parallel peripheral buses and data links	1031	15.8.1 Peripherals with direct connection	1079
14.7 Serial buses and data links	1032	15.8.2 Peripherals with SPI connection	1082
14.7.1 SPI	1032	15.8.3 Peripherals with I <sub>C</sub> connection	1084
14.7.2 I <sub>C</sub> 2-wire interface ("TWI")	1034	15.8.4 Some important hardware constraints	1086
14.7.3 Dallas-Maxim "1-wire" serial interface	1035	15.9 Development environment	1086
14.7.4 JTAG	1036	15.9.1 Software	1086
14.7.5 Clock-be-gone: clock recovery	1037	15.9.2 Real-time programming constraints	1088
14.7.6 SATA, eSATA, and SAS	1037	15.9.3 Hardware	1089
14.7.7 PCI Express	1037	15.9.4 The Arduino Project	1092
14.7.8 Asynchronous serial (RS-232, RS-485)	1038	15.10 Wrapup	1092
14.7.9 Manchester coding	1039	15.10.1 How expensive are the tools?	1092
14.7.10 Bipolar coding	1041	15.10.2 Where to use microcontrollers	1093
14.7.11 RLL binary-bit stuffing	1041	15.10.3 How to select a microcontroller	1094
14.7.12 RLL coding: 8B/10B and others	1041	15.10.4 A parting shot	1094
14.7.13 USB	1042	Review of Chapter 15	1095
14.7.14 FireWire	1042		
14.7.15 Controller Area Network (CAN)	1043		
14.7.16 Ethernet	1045		
14.8 Number formats	1046		
14.8.1 Integers	1046		
14.8.2 Floating-point numbers	1047		
Review of Chapter 14	1049		
<b>FIFTEEN: Microcontrollers</b>	<b>1053</b>		
15.1 Introduction	1053		
15.2 Design example 1: suntan monitor (V)	1054		
15.2.1 Implementation with a microcontroller	1054	<b>APPENDIX A: Math Review</b>	<b>1097</b>
15.2.2 Microcontroller code ("firmware")	1056	A.1 Trigonometry, exponentials, and logarithms	1097
15.3 Overview of popular microcontroller families	1059	A.2 Complex numbers	1097
15.3.1 On-chip peripherals	1061	A.3 Differentiation (Calculus)	1099
15.4 Design example 2: ac power control	1062	A.3.1 Derivatives of some common functions	1099
15.4.1 Microcontroller implementation	1062	A.3.2 Some rules for combining derivatives	1100
15.4.2 Microcontroller code	1064	A.3.3 Some examples of differentiation	1100
15.5 Design example 3: frequency synthesizer	1065		
15.5.1 Microcontroller code	1067	<b>APPENDIX B: How to Draw Schematic Diagrams</b>	<b>1101</b>
15.6 Design example 4: thermal controller	1069	B.1 General principles	1101
15.6.1 The hardware	1070	B.2 Rules	1101
15.6.2 The control loop	1074	B.3 Hints	1103
15.6.3 Microcontroller code	1075	B.4 A humble example	1103
		<b>APPENDIX C: Resistor Types</b>	<b>1104</b>
		C.1 Solid history	1104
		C.2 Available resistance values	1104
		C.3 Resistance marking	1105
		C.4 Resistor types	1105
		C.5 Confusion derby	1105
		<b>APPENDIX D: Thévenin's Theorem</b>	<b>1107</b>
		D.1 The proof	1107

14.11 Two examples – voltage dividers	1107	1.3 Recording analog-format broadcast or cable television	1135
14.12 Norton's theorem	1108	1.4 Digital television: what is it?	1136
14.13 Another example	1108	1.5 Digital television: broadcast and cable delivery	1138
14.14 Millman's theorem	1108	1.6 Direct satellite television	1139
<b>APPENDIX E: LC Butterworth Filters</b>	<b>1109</b>	1.7 Digital video streaming over internet	1140
E.1 Lowpass filter	1109	1.8 Digital cable: premium services and additional access	1141
E.2 Highpass filter	1109	1.8.1 Digital cable: video-on-demand broadcast	1142
E.3 Filter examples	1109	1.8.2 Digital cable: switched broadcast	1142
<b>APPENDIX F: Load Lines</b>	<b>1112</b>	1.9 Recording digital television	1142
F.1 An example	1112	1.10 Display technology	1142
F.2 Three-terminal devices	1112	1.11 Video connections: analog and digital	1143
F.3 Nonlinear devices	1113		
<b>APPENDIX G: The Curve Tracer</b>	<b>1115</b>	<b>APPENDIX J: SPICE Primer</b>	<b>1146</b>
J.1 Setting up ICAP SPICE	1146	J.1 Schematic entry	1146
J.2 Entering a Diagram	1146	J.3 Running a simulation	1146
J.3 Expanding the parts database	1149	J.4 Some final points	1148
H.1 Some properties of transmission lines	1116	J.5 A detailed example: exploring amplifier distortion	1148
H.1.1 Characteristic impedance	1116	J.6 Expanding the parts database	1149
H.1.2 Termination pulses	1117		
H.1.3 Termination: sinusoidal signals	1120	<b>APPENDIX K: "Where Do I Go to Buy Electronic Goodies?"</b>	<b>1150</b>
H.1.4 Loss in transmission lines	1121	J.3.1 Schematic entry	1146
H.2 Impedance matching	1122	J.3.2 Simulation: frequency sweep waveforms	1147
H.2.1 Resistive (lossy) broadband matching network	1123	J.3.3 Simulation: input and output waveforms	1147
H.2.2 Resistive attenuator	1123	J.4 Some final points	1148
H.2.3 Transformer (lossless) broadband matching network	1124	J.5 A detailed example: exploring amplifier distortion	1148
H.2.4 Reactive (lossless) narrowband matching networks	1125	J.6 Expanding the parts database	1149
H.3 Lumped-element delay lines and pulse-forming networks	1126		
H.4 Epilogue: ladder derivation of characteristic impedance	1127	<b>APPENDIX L: Workbench Instruments and Tools</b>	<b>1152</b>
H.4.1 First method: terminated line	1127	L.1 Workbench	1153
H.4.2 Second method: semi-infinite line	1127	L.2 Oscilloscope	1154
H.4.3 Postscript: lumped-element delay lines	1128	O.1 The analog oscilloscope	1158
		O.1.1 Vertical	1158
		O.1.2 Horizontal	1158
		O.1.3 Triggering	1159
I.1 Television: video plus audio	1131	O.1.4 Hints for beginners	1160
I.1.1 The audio	1131	O.1.5 Probes	1160
I.1.2 The video	1132	O.1.6 Grounds	1161
I.2 Combining and sending the audio + video modulation	1133	O.1.7 Other analog scope features	1161
		O.2 The digital oscilloscope	1162

O.2.1 What's different?	1162	APPENDIX P: Acronyms and Abbreviations	<b>1166</b>
O.2.2 Some cautions	1164		
Index			<b>1171</b>