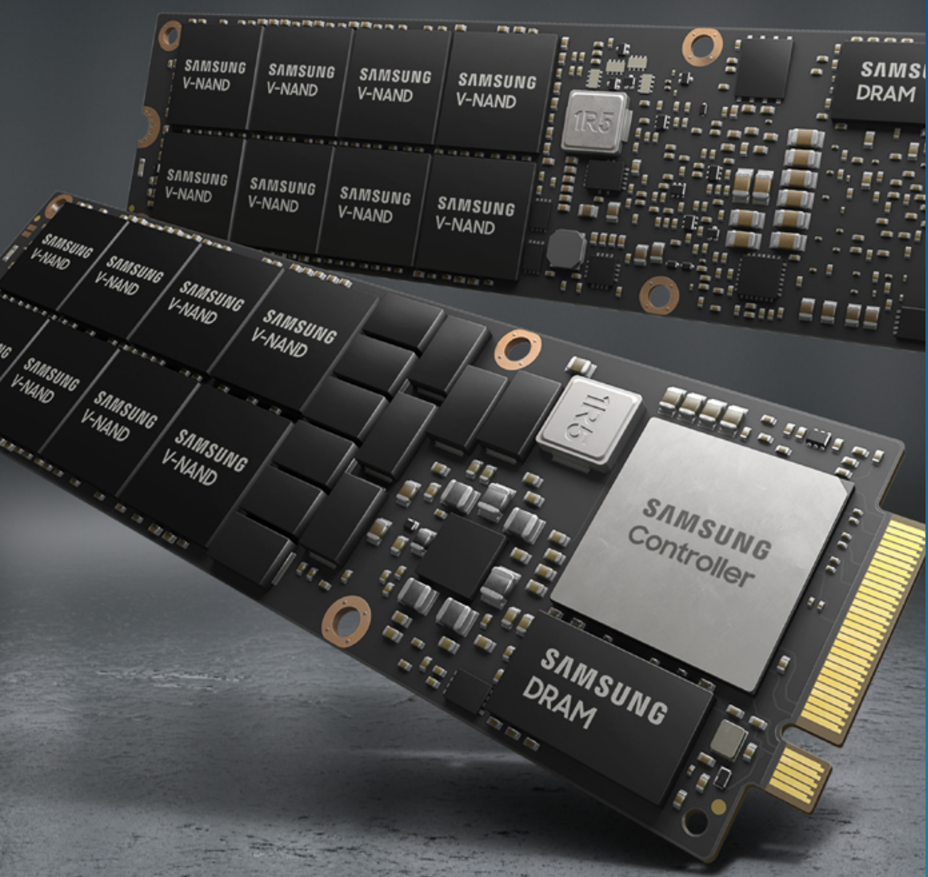

Samsung NGSFF SSD

State-of-the-Art SSD Solutions for Data Center and Enterprise Servers

White Paper

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The NGSFF SSD Value Proposition

Executive Summary

As the volume of global data grows dramatically each year, there is also an increasing demand for Solid State Drives (SSDs) that are optimized for data center and enterprise applications equipped with various features including higher density, hot plug support for front loading , and 12V power direct support, among others.

However, existing legacy SSD solutions, like U.2- and M.2-based SSDs, do not satisfiy such requirments from the data center and enterprise server industries. The U.2 form factor is still stuck to a 2.5-inch form factor, which originated with the spinning hard disk drive (HDD). Therefore the U.2 SSD is far from efficient when it comes to space usage, an attribute that is critical for data center and enterprise server applications. And, since M.2-based devices were invented primarily for consumer use, M.2-based solutions do not integrate key enterprise-level features, such as hot-swap, power loss protection, and higher capacity, even while its form factor cannot support the front drive loading on the server.

In order to solve these issues for the data center and enterprise industries, Samsung invented a new state-of-the-art SSD form factor targeted specifically for these applications – Next Generation Small Form Factor (NGSFF) [1]. This white paper will describe the key features and advantages of NGSFF SSDs in detail in order to help system vendors choose the right data center and enterprise server solutions to more efficiently run their businesses.

NGSFF SSD's 9 Advantages for Data Center and Enterprise Server Systems

NGSFF SSD is the way of the future for data centers and enterprise applications. The dimensions and key features are optimized to fully utilize the server front drive bay area space, helping to achieve a high density and space-efficient design. This results in the following key benefits for NGSFF SSDs:

- **(1) Double/quadruple capacity:** NGSFF form factor supports two-to-four times higher capacity than the M.2 form factor. Therefore, by using NGSFF SSDs, space utilization in regards to data center applications can be significantly improved.
- **(2) Universal form factor to support multiple SSD interface protocols, including PCIe, SAS, SATA and Gen-Z.**
- **(3) High Availability via a supporting Dual port:** For PCIe protocols, server systems can choose either a Single port x4 lane PCIe or Dual port x2 lane PCIe by setting the value of DualPortEn enable pin. This feature allows for multiple paths to the SSD, which is a critical feature for enterprise server systems. Even if one port is blocked due to a system or network issue, SSD data can still be accessed via the other port for continuous service.
- **(4) Hot-insertion/Hot-removal capabilities:** NGSFF SSDs can be replaced without a system power-off (i.e. replacing broken SSDs is easier and will not require stopping the server system).
- **(5) Server-front-bay serviceability:** With the feature of hot-insertion/hot removal, placing status LEDs in rear part and four screw holes for locking to the NGSFF SSD chassis make easier monitoring and safer insertion/removal of NGSFF SSD in the front-bay server.
- **(6) 12V power supply as the main power source for the SSD:** Because NGSFF SSDs can receive 12V voltage directly, server systems do not need to convert the voltage to 3.3V as the main power source of the SSD. The voltage regulator from 12V to 3.3V is not needed in the server system (i.e. voltage regulation related hardware and software are removed in the server system).
- **(7) Power reset capability by software:** The main power supply of 12V can be disabled while keeping the control signal like 3.3V aux active. This power disable capability allows easier remote power reset of the SSD by software.
- **(8) Power loss protection:** For sudden power loss protection, there is enough space for charge capacitors, which transfer cached data to the SSD. Therefore, the server host does not need to worry about losing data when power is lost.
- **(9) Visual reporting of detailed SSD status:** Two LEDs are included to provide the SSD status. Because these LEDs are placed in rear part of the NGSFF SSD, a system maintainer can easily monitor the NGSFF SSD's status.

The remainder of this white paper will explain these 9 key advantages of NGSFF SSDs in detail.

1. This state-of-the-art NGSFF SSD form factor design was invented by Samsung and introduced at the Flash Memory Summit (FMS) in 2016. The first NGSFF SSD product for use by the data center and enterprise server industries was announced at the 2017 FMS.

Mechanical Outline

Mechanical Outline and Higher Capacity

Figure 1 shows the shape of the NGSFF SSD form factor and its dimensions. Its outer size is 110.0mm by 30.5mm. The total thickness is 4.30mm or 4.8mm. The allowable component height for the top side is 2.0mm maximum, while the allowable component height for the bottom side is 1.50mm or 2.0mm maximum. The PCB thickness of the NGSFF SSD is 0.8mm with a ±10 % tolerance.

Figure 2 shows a NGSFF SSD product developed according to the NGSFF form factor specifications shown in Figure 1. The NGSFF SSD height of 30.5mm is optimally utilizing the 1U height of the server (i.e. 50% wider area than M.2 by increasing the height while not exceeding 1U height allows NGSFF SSDs to contain more semiconductor components in the same 1U Rack).

In comparison to the M.2 form factor-based SSD, NGSFF SSDs can have at least double the storage capacity because of a bigger PCB area (i.e. when using a JEDEC standard NAND package--14x18mm, 316BGA--8 NAND packages can be mounted on the NGSFF SSD form factor, while only up to 4 NAND packages can be mounted on a M.2 form factor).

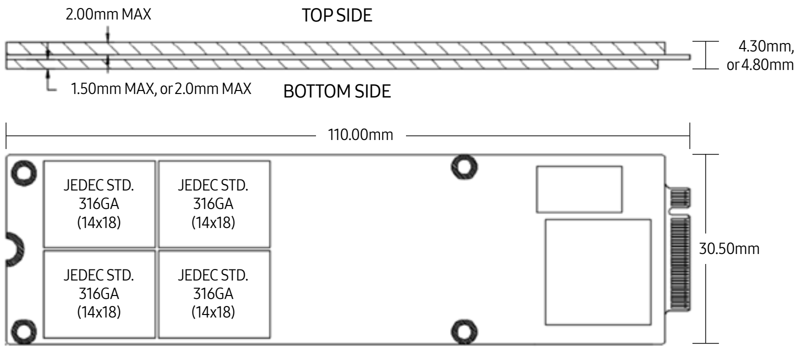

Figure 1 - NGSFF SSD Mechanical Dimensions

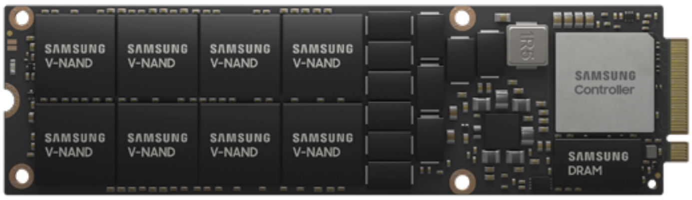

Figure 2 - NGSFF SSD (30.5x110mm) Mounting Two Rows of Eight NANDs
(Using Both Sides of PCB, a Total of 16 NANDs Are Mounted)

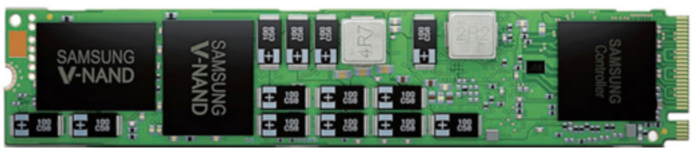

Figure 3 - M.2 SSD (22x110mm) Mounting Only One Row of Two NANDs
(Using Both Sides of PCB, a Maximum 4 NANDs Are Mounted)

If a current, widely-used, smaller size NAND Package (12.7x13.1mm) is used (as shown in Figure 2), a total of 16 NAND packages can be mounted on a NGSFF SSD. Using a NGSFF SSD can provide 4 times higher storage capacity than an M.2-based server system. This reduces the rack space of a data center dramatically. For example, one rack of a NGSFF SSD can replace four racks of an M.2-based SSD in a data center while providing the same total storage capacity with less power consumption.
As shown in Figure 4, each 1U rack unit can easily fit 36 NGSFF SSDs. For instance, if Samsung's PM983 16TB NGSFF NVMe SSD is used, then 576TB of system capacity is provided using only a 1U server.

Figure 4: 36 NGSFF SSDs--Samsung's PM983 16TB NGSFF NVMe SSD--Can Fit Into a Current 1U Server; 576TB of System Capacity Can Be Provided Per One 1U Rack Unit

Server-Front-Bay Serviceability

Simplifying Maintenance Via Server-Front-Bay Serviceability

The NGSFF form factor is designed with features like hot insertion, hot removal, activity and status indicator LEDs. Collectively, these features enable the NGSFF SSD to be usable and serviceable from the front bay of standard 1U servers. The following figure shows the insertion of an NGSFF SSD to a 1U server drive bay.

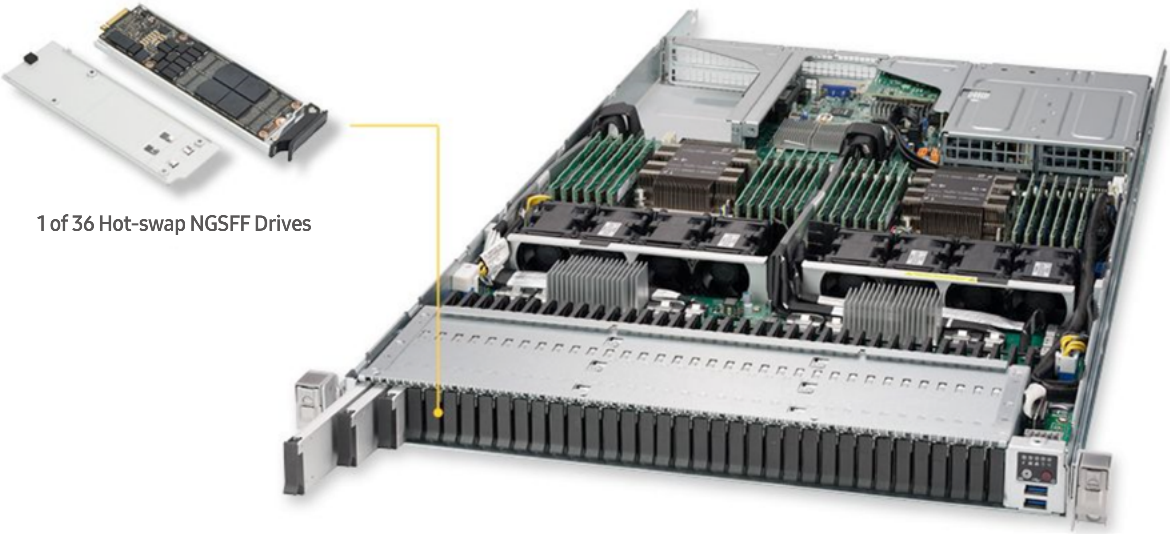

Figure 5: Server Front-Bay Serviceability of NGSFF SSD

Universal Form Factor to Support PCIe, SAS and SATA Interfaces

The NGSFF form factor is designed to support multiple bus interfaces, including PCIe [2], SATA [3] and SAS [4]. In cases where the interface detect signal (IfDET, Pin 69) is GND, NGSFF SSDs will follow the SAS or SATA protocol. If the interface detect signal (IfDET, Pin 69) is high in conjunction with a platform located pull-up resistor, the device protocol is PCIe. In the case of PCIe interface type, if DualPortEn# value is set High by system, then the device will operate in Single port 4 lanes PCIe protocol. Otherwise, the PCIe interface is working as Dual port 2 lanes PCIe protocol (see Table 1).

SSD Interface Type	IfDET (Pin 69, Output)	DualPortEn# (Pin46, Input)
SATA or SAS	GND	Open
PCIe (Single port)	Open	High (by system)
PCIe (Dual port)	Open	Low (by system)

Table 1: Protocol Type Identification

2. PCIe: PCI Express interface protocol, which is defined by PCI SIG (http://pcisig.com/).
3. SATA: SATA (Serial ATA) is a computer bus interface used for mass storage devices such as HDDs and defined by the Serial ATA international organization (http://www.serialata.org/).
4. SAS: SAS (Serial Attached SCSI) is a bus interface used for mass storage devices such as HDDs and defined by the T10 technical committee (http://www.t10.org/).

Supporting multiple SSD protocols

Table 2 shows the Pin out allocation when NGSFF SSDs interface in the PCIe Single port x4 lane. Signals with blue colored background (52-55, 49-50, 47, 43, 41, 37, 35, 31, 29, 25, 23, 19, 17, 13, 11, 7 and 5) are used for the Single port x4 Lane PCIe protocol.

If the interface detect signal (IfDET) is low, then the interface protocol of the NGSFF SSD is SAS or SATA. Since the identification of SAS or SATA is done by software, the same scheme used in the traditional way can be applied (please refer to the appendix part of this white paper for the Pin out allocation when the NGSFF SSD interface is SATA or SAS).

Dual Port Support for PCIe

The PCI Express (PCIe) interface may be configured as either a Single port x4 lane SSD or a Dual port x2 lane SSD. If the dual port control signal, called DualPortEn# (Pin 46), is enabled by the host then the NGSFF SSD works as a Dual port x2 lane mode to provide High Availability, which is needed by many enterprise server systems.
In Table 3, signals with purple colored background (48, 46, 24 ~ 22, 17, 19, 13, 11, 7 and 5) are used for the second port of the x2 Lane PCIe protocol.

Mating Group	Pin	Signal	Signal	Pin	Mating Group
			GND	75	1st
2nd	74	N/C	GND	73	1st
2nd	72	N/C	GND	71	2nd
2nd	70	N/C	IfDET (NC)	69	2nd
2nd	68	Reserved	PRSNT1#	67	2nd
	66	Module Key	Module Key	65	
	64	Module Key	Module Key	63	
	62	Module Key	Module Key	61	
	60	Module Key	Module Key	59	
2nd	58	Reserved for MFG_CLOCK	GND	57	2nd
2nd	56	Reserved for MFG_DATA	A-REFCLKp	55	2nd
2nd	54	PEWAKE#	A-REFCLKn	53	2nd
2nd	52	CLKREQ#	GND	51	2nd
2nd	50	A-PERST#	Rx+0	49	2nd
2nd	48	N/C	Rx-0	47	2nd
2nd	46	N/C	GND	45	2nd
2nd	44	ALERT#	Tx+0	43	2nd
2nd	42	SMB_DATA	Tx-0	41	2nd
2nd	40	SMB_CLK	GND	39	2nd
2nd	38	N/C	Rx+1	37	2nd
1st	36	12V (Pre-Charge)	Rx-1	35	2nd
2nd	34	12V	GND	33	2nd
2nd	32	12V	Tx+1	31	2nd
2nd	30	12V	Tx-1	29	2nd
1st	28	PWDIS	GND	27	2nd
2nd	26	GND	Rx+2	25	2nd
2nd	24	N/C	Rx-2	23	2nd
2nd	22	N/C	GND	21	2nd
2nd	20	GND	Tx+2	19	2nd
2nd	18	N/C	Tx-2	17	2nd
2nd	16	N/C	GND	15	2nd
2nd	14	N/C	Rx+3	13	2nd
2nd	12	3.3Vaux	Rx-3	11	2nd
2nd	10	LED	GND	9	2nd
2nd	8	NC	Tx+3	7	2nd
2nd	6	PRSNT2#	Tx-3	5	2nd
2nd	4	N/C	GND	3	1st
2nd	2	N/C	GND	1	1st

Table 2: NGSFF SSD PCIe Single port x4 Lane Interface Pinout

Mating Group	Pin	Signal	Signal	Pin	Mating Group
			GND	75	1st
2nd	74	N/C	GND	73	1st
2nd	72	N/C	GND	71	2nd
2nd	70	N/C	IfDET (NC-PCIe)	69	2nd
2nd	68	Reserved	PRSNT1#	67	2nd
	66	Module Key	Module Key	65	
	64	Module Key	Module Key	63	
	62	Module Key	Module Key	61	
	60	Module Key	Module Key	59	
2nd	58	Reserved for MFG_CLOCK	GND	57	2nd
2nd	56	Reserved for MFG_DATA	A-REFCLKp	55	2nd
2nd	54	PEWAKE#	A-REFCLKn	53	2nd
2nd	52	CLKREQ#	GND	51	2nd
2nd	50	A-PERST#	Rx+0	49	2nd
2nd	48	B-PERST#	Rx-0	47	2nd
2nd	46	DualPortEn#	GND	45	2nd
2nd	44	ALERT#	Tx+0	43	2nd
2nd	42	SMB_DATA	Tx-0	41	2nd
2nd	40	SMB_CLK	GND	39	2nd
2nd	38	N/C	Rx+1	37	2nd
1st	36	12V (Pre-Charge)	Rx-1	35	2nd
2nd	34	12V	GND	33	2nd
2nd	32	12V	Tx+1	31	2nd
2nd	30	12V	Tx-1	29	2nd
1st	28	PWDIS	GND	27	2nd
2nd	26	GND	Rx+2	25	2nd
2nd	24	B-REFCLKp	Rx-2	23	2nd
2nd	22	B-REFCLKn	GND	21	2nd
2nd	20	GND	Tx+2	19	2nd
2nd	18	N/C	Tx-2	17	2nd
2nd	16	N/C	GND	15	2nd
2nd	14	N/C	Rx+3	13	2nd
2nd	12	3.3Vaux	Rx-3	11	2nd
2nd	10	LED	GND	9	2nd
2nd	8	NC	Tx+3	7	2nd
2nd	6	PRSNT2#	Tx-3	5	2nd
2nd	4	N/C	GND	3	1st
2nd	2	N/C	GND	1	1st

Table 3: NGSFF SSD PCIe Dual port x2 Lane Interface Pinout

12V Direct Main Power support

Gen-Z Interface Support

Gen-Z [5] supports a wide range of physical layer signaling rates and types, including both electrical and optical. NGSFF SSDs may support Gen-Z devices that utilize the PCIe physical layer. The Gen-Z device appears to the system as a PCIe device before and during training.

12V Direct Main Power and 3.3V Aux Power

The NGSFF supports 12V as the main power source (Pin 30, 32, 34, 36) to the SSD. Therefore, the host does not need to convert from 12V to 3.3V voltage in the host system. Therefore, the number of voltage regulator chips on the host system PCB is reduced. This decreases the complexity of the PCB and software while lowering the BOM cost as well. One of the 12V pins (pin 36, pre-charge) is defined as the first mating group pin, which should be connected to the host system first. This is to extract remaining electrons in order to avoid sparking. As a result, hot-plug insertion can be performed safely in the system level.

NGSFF also supports 3.3V aux power sources (pin 12) in order to provide power to supported sideband communications. Even though the SSD is powered off for power saving, SM bus can work based on 3.3Vaux power. Therefore, basic information like SSD capacity, temperature and other details, can be read by host system.
Table 4 describes the electrical requirements of 12V and 3.3V power sources.

Power Rail	Requirement
12V (main power source for SSD) - Maximum power - Voltage tolerance - Max continuous current1 - Max peak current[2]	16W (max) ±8% 1.3A (max) 2.0A (max)
3.3V (for side band) - Voltage tolerance - Max continuous current3	±8% 1mA (max)

Note 1: Maximum continuous current is defined as the highest average current value over a one second period. This is the sum of all the pins.
Note 2: Maximum current to limit connector damage and limit instantaneous power.
Note 3: Maximum continuous current is defined as the highest average current value over a one second period. This is the sum of all the pins.

Table 4: Power Supply Rail Requirements

Power Reset of NGSFF SSD by Software

NGSFF supports a "Power Disable" control signal, called PWDIS (Pin 28), which disables 12V power to all of the active components on the NGSFF SSD. This PWDIS functionality is applied only to the 12V supply, and does not affect the 3.3V supply. Therefore, this control signal can be utilized to power off most SSD components based on 12V while keeping minimum control capabilities based on 3.3V Aux power source. This power disable capability allows for easier remote power reset of SSD by software.

Since this PWDIS control signal is used to control supplying 12V power to the device, this pin is defined as the 1st mating group pin, which should be connected to the host first.

5. Gen-Z offers a universal interface for compute, memory, storage, and I/O and supports local and shared storage. Gen-Z block storage can be mapped and viewed like any other PCIe block storage device (https://genzconsortium.org/).

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Hot-Plug Insertion and Removal

Hot-Plug Insertion and Removal and Host-Side Implementation

To support hot-insertion and hot-removal of the NGSFF SSD, the two presence detect signals--PRSNT 1# (pin 67) and PRSNT 2# (pin 6)--are defined. These presence detect signals are used by the system to recognize the presence of an NGSFF SSD in order to enable auxiliary signals like the reference clock, PCIe reset, and SMBus signals.

On the NGSFF SSD, the presence detect pins are connected with a trace so that PRSNT 1# is electrically connected to PRSNT 2# on the host platform when the NGSFF SSD is inserted into the connector.

Figure 6 shows an example of how the host system can detect the NGSFF SSD insertion using PRSNT 1# and PRSNT 2#. According to the host implementation example in Figure 6, if the NGSFF SSD is inserted, the hot-plug detection logic detects the change of voltage level as GND level, and host system may start the initialization procedure. If the NGSFF SSD is removed, then the hot-plug detection logic detects the change of voltage level as pull-up voltage level, and the host system will stop signaling and power supply.

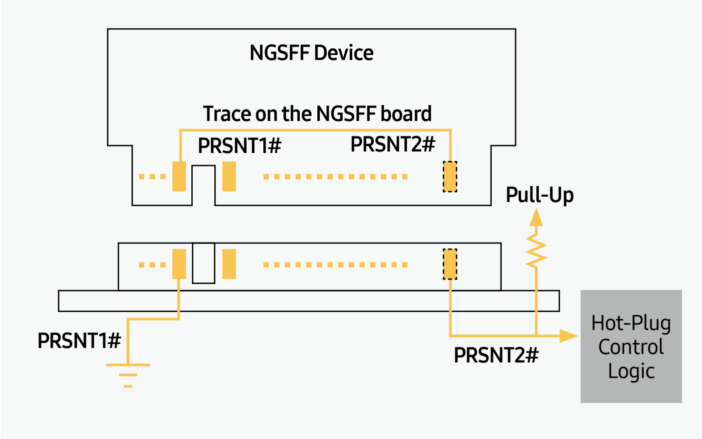

Figure 6: An Example of Host-Side Implementation for Hot-Plug Support Using PRSNT#1/#2

First Mating Group Pins and Host-Socket Implementation Example

Since the 12V (pre-charge, pin 36) and PWDIS (pin 28) should be detected first by the host, these signals are defined as the 1st mating group signal. The host socket connector should be designed for the 1st mating group signals to be connected first with the host system.

Figure 6 is a cross-section drawing of an NGSFF SSD connector. Connector pins are organized in a staggered arrangement depending on the mating group in order to enable signal connections at different times during the module insertion process. Due to the staggered connector pin arrangement on the NGSFF SSD connector, six pins (GND, 12V pre-charge, PWDIS pins) shall be mated to the gold fingers of NGSFF SSD earlier than other pins during the module insertion process. The first mated signal pins are pins 1, 3, 73, and 75 on the top-side and pins 28 and 36 on the bottom-side. All other signal pins belong to the second mated pin group.

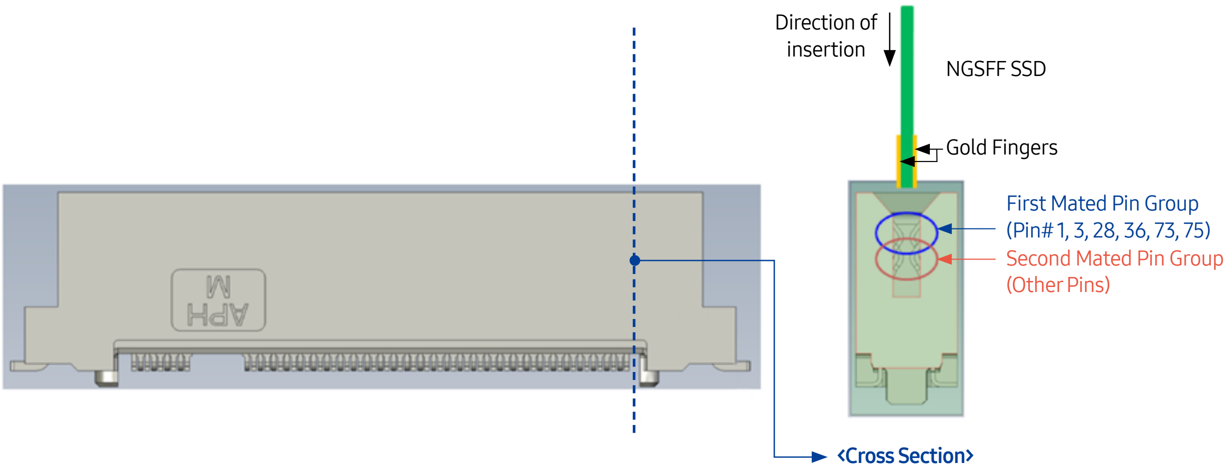

Figure 7: An Example of a Staggered Socket Contact Arrangement for 1st Mating Pins to Be Connected First (Cross-Section Drawing of NGSFF SSD Connector)

Status Reporting of NGSFF SSD

Visual Reporting of SSD Status

Two status indicator LEDs are mounted on the rear part of the NGSFF SSD in order for the server maintainer to monitor the status of the NGSFF SSD easily and visually. Lighting of both LEDs are driven by the internal controller of the SSD. Figure 8 illustrates the placement of the LEDs on the NGSFF SSD. When it is inserted into the NGSFF SSD in the front bay of a standard 1U server, the LED lights are easy to monitor.

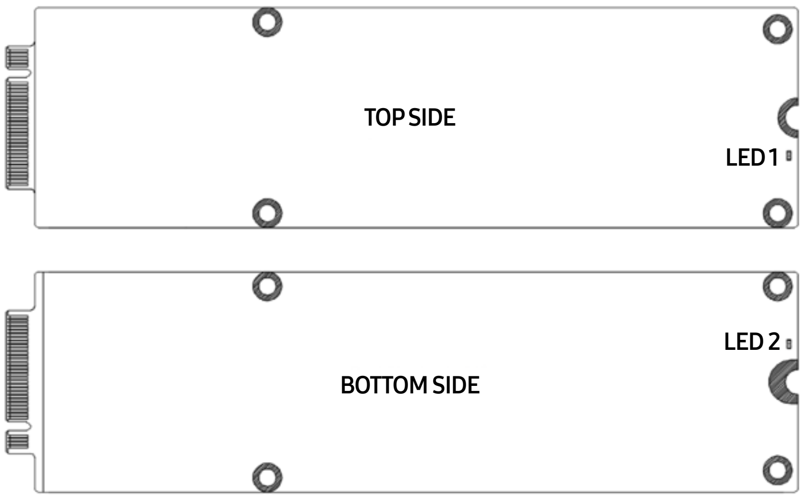

Figure 8: LED Locations on NGSFF Form Factor

Table 5 shows an example of the status LED light patterns, sequences, and respective meanings. Please note, the definition of the pattern and sequences of the status indicator LED light is implementation specific, established at the discretion of the system designer, and supported by specific SSD implementations.

LED	Condition	Activity
LED1 (Amber) Service Action	Drive healthy, or slot power off	OFF
	Drive fault	Steady ON
LED2 (Green) Activity Signal	Drive not operational, or power-off	OFF
	Drive operational, no activity, no fault	Steady ON
	Drive operational, Read/Write activity	Activity Blink

Table 5: An Example of LED Lights for Reporting NGSFF SSD Status

Interface Signals

Electrical Specifications

Note that the signal name is defined from the perspective of the SSD device (i.e. the Rx or input signal means the receiving signal is from the SSD device's perspective and not from the host's point of view).

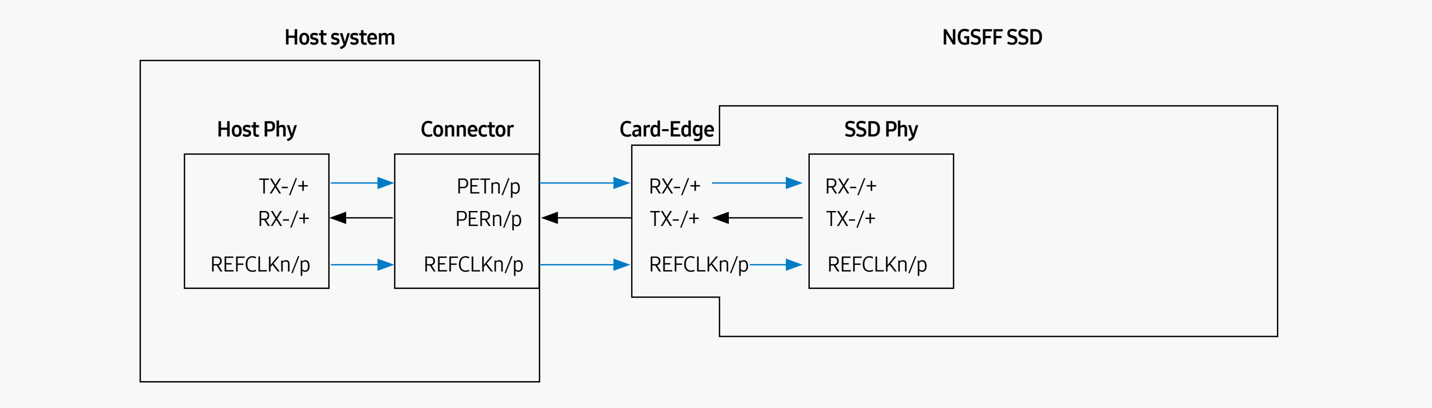

Figure 9: NGSFF SSD Signal Naming Conventions

Table 6 shows the list of the NGSFF SSD interface signals.

Interface	Name	Type	Function	Voltage
Power and Ground	12V	Input	12V Source; 4 pins	12V
	GND	-	Return current path; 16 pins	0V
	3.3V	Input	3.3V AUX Power (Optional)	3.3V
PCIe High Speed	Rx+0, Rx-0, Tx+0, Tx-0, Rx+1, Rx-1, Tx+1, Tx-1, Rx+2, Rx-2, Tx+2, Tx-2, Rx+3, Rx-3, Tx+3, Tx-3	Input/ Output	PCIe x4 Transmit and Receive signal. The interface may be configured as Single port x4, or Dual port x2. Rx: Device Receiver differential signal Tx: Device Transmitter differential signal	
PCIe Side Band	A-REFCLKp, B-REFCLKn	Input	PCIe Reference Clock (for port A) 100MHz	
	A-PERST#	Input	PCIe Reset (Port A) is the functional pin to reset the module	
Dual port PCIe Side Band	B-REFCLKp B-REFCLKn	Input	PCIe Reference Clock (for Port B in case of Dual mode) 100MHz	
	B-PERST#	Input	PCIe Reset (Port B) is the functional pin to reset the module	
	DualPortEn#	Input	Enable Dual-port mode. The DualPortEn# signal is pulled high internally to an NGSFF SSD. If the DualPortEn# signal is not actively driven lower by the host system, then the NGSFF SSD is configured as a single port x4 lane SSD. If the DualPortEn# is pulled low by the host system, then the NGSFF SSD is configured as a Dual port x2 lane SSD. DualPortEn# is a static signal. DualPortEn# must be stable for1 us before either A-PERST# or B-PERST# are de-asserted, and the DualPortEn# can only change if both A-PERST# and B-PERST# are asserted.	
PCIe Optional Sideband	CLKREQ#	Input/ Output	Reference clock request signal	
	PEWAKE#	Input/ Output	PCIe WAKE# signal for link reactivation Open drain with pull up on platform. Active Low signal.	

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Interface Signals

SATA	Rx+0,Rx-0, Tx+0,Tx-0,	Input/ Output	SATA Transmit and Receive signal Rx: Device Receiver differential signal Tx: Device Transmitter differential signal	
SATA Sideband	DEVSLP	Input	Host-controlled signal which tells the device to enter the low power state, called DevSleep mode. For DevSleep details, refer the Serial ATA Specification Revision 3.3.	
	DAS	Output	Device Activity Signal (DAS). The device provides the DAS signal for activity indication. Open Drain, Active Low signals. For more details, refer the Serial ATA Specification Revision 3.3.	3.3V
SAS x4 High Speed	Rx+0, Rx-0, Tx+0, Tx-0, Rx+1, Rx-1, Tx+1, Tx-1, Rx+2, Rx-2, Tx+2, Tx-2, Rx+3, Rx-3, Tx+3, Tx-3-	Input/ Output	SAS x4 Transmit and Receive signal Rx: Device Receiver differential signal Tx: Device Transmitter differential signal	
Shared Support	IfDET	Output	Interface Detect. Drive type encoded on IfDET by the device. (SATA/SAS if IfDET is GND; PCIe if IfDET is NC)	
	LED	Output	LED signal provides SSD status indications via platform provided indicators Open Drain, Active Low signals SAS devices use the pin for READY LED signal	3.3V
	ALERT#	Output	Alert notification to host system. Open Drain with pull up on platform; Active Low Signals	3.3V
	SMB_CLK	Input/Output	SMBus clock; Open drain with pull up on platform	3.3V
	SMB_DATA	Input/Output	SMBus Data; Open drain with pull up on platform	3.3V
	PWDIS	Input	Power Disable Signal: PWDIS disables 12V power to all of the active components on the NGSFF SSD. The NGSFF SSD shall support PWDIS. Support of PWDIS is optional for the system board. The characteristics of PWDIS shall comply with the characteristics defined in the respective interface specification supported by the NGSFF SSD. PWDIS functionality is applied only to the 12V supply, and does not affect the availability of 3.3 Vaux.	3.3V
	PRSNT1#/ PRSNT 2#	-	Presence Detect. The NGSFF SSD shall support Hot-Plug/Hot-Removal. However, hardware support of Hot-Plug/Hot-Removal on the system board is optional.	
	Reserved for MFG_CLOCK	Input	Manufacturing DATA and CLOCK lines. Used only in the SSD manufacturing stage.	
	Reserved for MFG_DATA	Input/Output		

Table 6: NGSFF SSD Interface Signals

Summary

This white paper outlined the reasons why legacy form factor U.2- and M.2-based SSDs are not sufficient for enterprise and data center server systems.

To provide a solution, Samsung invented a new SSD form factor called NGSFF which is optimized for enterprise and data center server applications. NGSFF delivers the following key 9 advantages for such server systems:

1) Can provide 2 ~ 4 times higher capacity than M.2-based solutions, which dramatically improves space utilization in data center applications.
2) Offers support for multiple SSD interface protocols, including PCIe, SAS, SATA, Gen-Z.
3) High Availability by supporting Dual port for PCIe.
4) Hot-insertion and Hot-removal capabilities allowing for SSD replacement to be conducted without system power-off.
5) Server-front-bay serviceability allowing the system maintainer's SSD replacement work to be done more easily.
6) 12V power supply for main power of SSD, eliminating the need for a voltage regulator.
7) Power reset capability via software.
8) For sudden power loss case, enough space for charge capacitors is provided.
9) Visual Reporting of SSD Status using two LEDs in the rear part of NGSFF for easier monitoring.

Samsung's NGSFF SSD products were already released as PM983 NGSFF NVMe SSD with capacities of 16TB, 8TB and 4TB. In addition, the NGSFF Reference Server System was also developed to demonstrate the NGSFF SSD's 9 advantages and Samsung has published the Reference Server Design Guidelines for NGSFF SSD. Please contact Samsung to purchase PM983 NGSFF NVMe SSD products and obtain technical support for building enterprise and data center server systems.

Appendix A: Pinout and Signal Name

Table A.1 and Table A.2 provide a list of signal pinouts when the NGSFF SSD interface is SAS x4 lanes (Table A.1) and SATA x4 lanes (Table A.2).

Mating Group	Pin#	Signal	Signal	Pin#	Mating Group
			GND	75	1st
2nd	74	N/C	GND	73	1st
2nd	72	N/C	GND	71	2nd
2nd	70	N/C	IfDET (GND)	69	2nd
2nd	68	Reserved	PRSNT1#	67	2nd
	66	Module Key	Module Key	65	
	64	Module Key	Module Key	63	
	62	Module Key	Module Key	61	
	60	Module Key	Module Key	59	
2nd	58	Reserved for MFG_CLOCK	GND	57	2nd
2nd	56	Reserved for MFG_DATA	N/C	55	2nd
2nd	54	N/C	N/C	53	2nd
2nd	52	N/C	GND	51	2nd
2nd	50	N/C	Rx+0	49	2nd
2nd	48	N/C	Rx-0	47	2nd
2nd	46	N/C	GND	45	2nd
2nd	44	ALERT#	Tx+0	43	2nd
2nd	42	SMB_DATA	Tx-0	41	2nd
2nd	40	SMB_CLK	GND	39	2nd
2nd	38	N/C	Rx+1	37	2nd
1st	36	12V (Pre-Charge)	Rx-1	35	2nd
2nd	34	12V	GND	33	2nd
2nd	32	12V	Tx+1	31	2nd
2nd	30	12V	Tx-1	29	2nd
1st	28	PWDIS	GND	27	2nd
2nd	26	GND	Rx+2	25	2nd
2nd	24	N/C	Rx-2	23	2nd
2nd	22	N/C	GND	21	2nd
2nd	20	GND	Tx+2	19	2nd
2nd	18	N/C	Tx-2	17	2nd
2nd	16	N/C	GND	15	2nd
2nd	14	N/C	Rx+3	13	2nd
2nd	12	3.3Vaux	Rx-3	11	2nd
2nd	10	LED	GND	9	2nd
2nd	8	NC	Tx+3	7	2nd
2nd	6	PRSNT2#	Tx-3	5	2nd
2nd	4	N/C	GND	3	1st
2nd	2	N/C	GND	1	1st

Table A.1: NGSFF SSD SAS x4 Lane Interface Pinout

Mating Group	Pin#	Signal	Signal	Pin#	Mating Group
			GND	75	1st
2nd	74	N/C	GND	73	1st
2nd	72	N/C	GND	71	2nd
2nd	70	N/C	IfDET (GND)	69	2nd
2nd	68	Reserved	PRSNT1#	67	2nd
	66	Module Key	Module Key	65	
	64	Module Key	Module Key	63	
	62	Module Key	Module Key	61	
	60	Module Key	Module Key	59	
2nd	58	Reserved for MFG_CLOCK	GND	57	2nd
2nd	56	Reserved for MFG_DATA	N/C	55	2nd
2nd	54	N/C	N/C	53	2nd
2nd	52	N/C	GND	51	2nd
2nd	50	N/C	Rx+0	49	2nd
2nd	48	N/C	Rx-0	47	2nd
2nd	46	N/C	GND	45	2nd
2nd	44	ALERT#	Tx-0	43	2nd
2nd	42	SMB_DATA	Tx+0	41	2nd
2nd	40	SMB_CLK	GND	39	2nd
2nd	38	DEVSLP	N/C	37	2nd
1st	36	12V (Pre-Charge)	N/C	35	2nd
2nd	34	12V	GND	33	2nd
2nd	32	12V	N/C	31	2nd
2nd	30	12V	N/C	29	2nd
1st	28	PWDIS	GND	27	2nd
2nd	26	GND	N/C	25	2nd
2nd	24	N/C	N/C	23	2nd
2nd	22	N/C	GND	21	2nd
2nd	20	GND	N/C	19	2nd
2nd	18	N/C	N/C	17	2nd
2nd	16	N/C	GND	15	2nd
2nd	14	N/C	N/C	13	2nd
2nd	12	3.3Vaux	N/C	11	2nd
2nd	10	DAS	GND	9	2nd
2nd	8	N/C	N/C	7	2nd
2nd	6	PRSNT2#	N/C	5	2nd
2nd	4	N/C	GND	3	1st
2nd	2	N/C	GND	1	1st

Table A.2: NGSFF SSD SATA x4 Interface Pinout

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